AND8309/D

Trends in Integrated Circuits that Affect ESD Protection Requirements

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Integrated Circuit Trends

The stunning progress in integrated circuit capability over the last 40 years is most succinctly expressed by Moore's Law; "Every 2 years the number of transistors that can be economically manufactured in an integrated circuit will double". The secret to this success has been the shrinking of integrated circuit feature sizes in all three dimensions. To maintain circuit reliability with the smaller dimensions the operating voltage of integrated circuits has been steadily declining. This trend will continue in the future, as documented in the International Technology Roadmap for Semiconductors (International Technology Roadmap for Semiconductors', http://www.itrs.net, 2000–2006), Figure 1. As the working voltage for integrated circuits decreases the voltage at which circuit damage can occur also decreases.

The move to smaller geometries has also prompted fundamental changes in IC technologies that have had an adverse effect on the intrinsic ability of the technologies to survive ESD stress. A prime example is the evolution of nMOS transistors in CMOS technologies. Some of the changes that have degraded the nMOS's ability to survive ESD are outlined in Table 1.

Table 1. nMOS INNOVATIONS IN CMOS TECHNOLOGY

Change	Reason for Implementation	Impact on ESD
Shallower Junctions	Allows Shorter Channel Length Transistors	Higher Current Density During an ESD Event
Lightly Doped Drains	Reduce Hot Carrier Transistor Degradation	Degraded Performance of Parasitic Bipolar Transistor which Provides Intrinsic High Current Capability
Silicided Junctions	Reduced Transistor Series Resistance	Removes Ballast Resistance in nMOS Drains, Degrading High Current Carrying Capability of Parasitic Bipolar Transistor
Thin Gate Oxides	Improved Transistor Performance	Reduced Voltage at Which Oxide Damage Occurs

The overall effect of technology changes on the ESD robustness of integrated circuits is discussed in the "Electrostatic Discharge (ESD) Technology Roadmap" produced by the Electrostatic Discharge Association (ESDA) (see Electrostatic Discharge (ESD) Technology Roadmap, ESD Association, 7900 Turin Rd. Bldg. 3, Rome NY 13440, 2005). This document shows the history and future trends in robustness of integrated circuits to ESD. An example for Human Body Model (HBM) robustness is shown in Figure 2. The HBM trend, and similar trends for Charged Device Model (CDM) and Machine Model (MM), point out an important development. In the 1980s and into the 1990s integrated circuits became more robust, even in a period of rapidly shrinking IC geometries. This reflected improved understanding of how to design ESD protection into ICs. In the late 1990s and into the 21st century the shrinking of IC geometries has outpaced innovative technology to provide on chip protection leaving IC's more vulnerable to damage from ESD.

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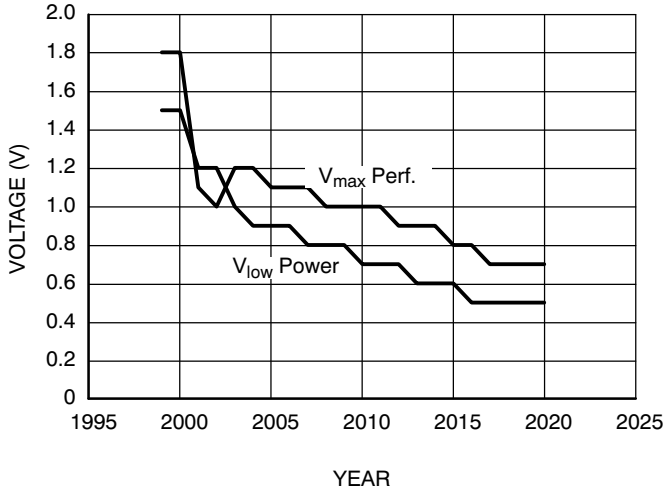

Figure 1. Operating voltage for advanced ICs from the International Technology Roadmap for Semiconductors. Values from 1999 to 2006 were taken from that year's roadmap. Values for 2007 through 2020 were taken from the 2006 update.

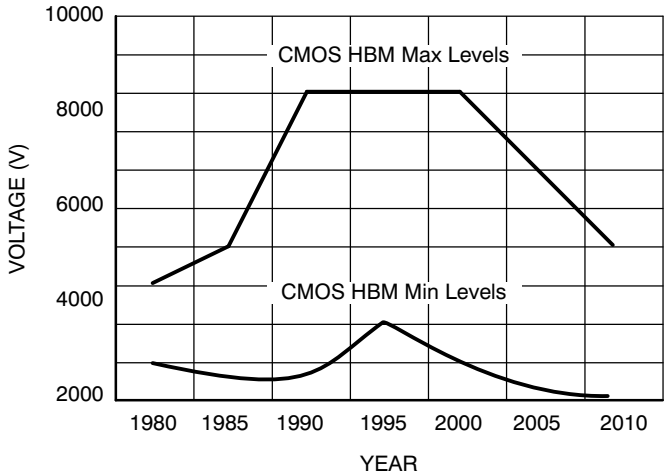

Figure 2. Human Body Model Sensitivity Limits based on ANSI/ESD STM5.1

Effect of IC Trend on System Level ESD

Lower working voltages and reduced device level ESD robustness has an effect on the requirements for external ESD protection components. ESD testing of ICs to the HBM, CDM and MM standards indicate an IC's ability to survive circuit board and system assembly in ESD controlled environments. System level ESD tests, such as IEC 61000−4−2, are much more severe than the device level tests. Electronic systems, such as laptops and mobile phones, must therefore be capable of providing off−chip ESD protection for ICs within the system.

System level ESD protection is provided in a number of ways. The system case provides physical protection and shielding and good board design can direct many ESD threats to system ground rather than to sensitive circuit elements. These design elements can not fully prevent ESD threats from getting coupled into sensitive IC's, though. Protection elements located at sensitive nodes are and effective solution to divert harmful ESD events away from IC's. Protection elements must be matched to the circuits they are protecting. All IC pins have an intended voltage range for operation, as illustrated in Figure 3. Beyond the intended voltage range is a safe guard band. Voltage beyond the guard band will initiate circuit damage. As more advanced technologies are used, and the operating voltage is decreased, the width of the guard band region also decreases. ESD protection components need to work within the guard band as shown in Figure 3. A narrower guard band requires protection elements with lower resistance in their "on" state resulting in lower ESD clamping voltages to prevent voltage excursions from getting into the device damage region. ON Semiconductor recognizes this requirement and designs their ESD protection solutions to have industry leading low clamping voltage.

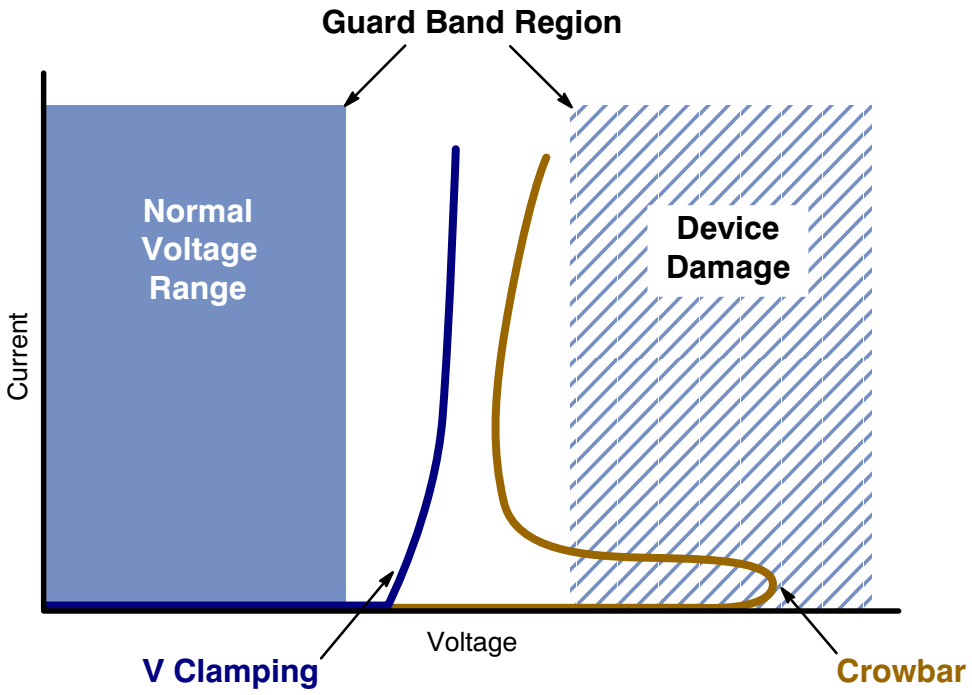

Figure 3. Operation of ESD Protection Components

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